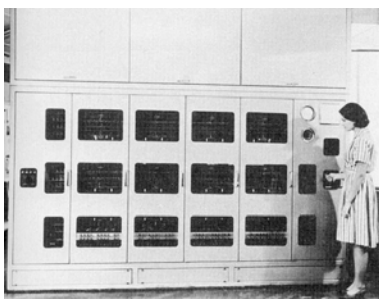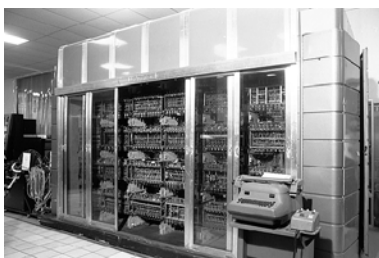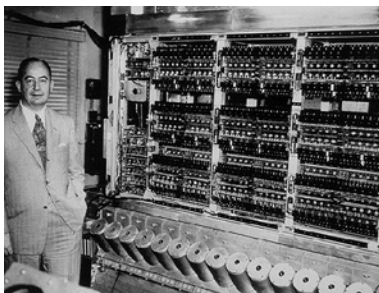# The IAS Computer Family Scrapbook

18 handbuilt
computers and
29 production line
models from

USA,
Sweden,
Israel,
Australia,
Japan,
Denmark

& some cousins
ARRA II
FERTA
GEORGE
MERLIN
R1

AVIDAC
BESK
CYCLONE
DASK
EDB
FACOM 201
IBM 701
ILLIAC
JOHNNIAC
MANIAC
MISTIC
MUSASINO
ORACLE
ORDVAC
SARA
SILLIAC
SMIL
TRASK
WEIZAC

by John Deane

AUSTRALIAN COMPUTER MUSEUM SOCIETY

The IAS Computer Family Scrapbook

by John Deane

The "IAS Family" is more formally known as
Princeton Class machines
(the *Institute for Advanced Study* is at Princeton, NJ, USA), and they were referred to as
JONIACs
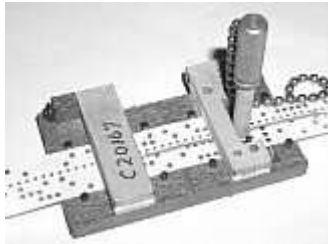by Klara von Neumann in her forward to her husband's book *The Computer and the Brain*.

IAS computer family prime programming terminal

Table of Contents

These are listed in order of completion. Of these
- the first to run was ORDVAC in 1951 and TRASK the last in 1965,
- the most unusual may be MUSACHINO-1 based on *parametron* devices,
- or TRASK built from transistors (the rest used vacuum tubes),
- the earliest demise was AVIDAC in 1957,
- and the latest was TRASK in 1980 – but that's cheating, it used transistors,
- the latest vacuum tube machine was probably SMIL in 1970 (but not all dates are in),
- longest lived may be ORDVAC at 16 years (but that's not verified),
- again TRASK comes in at 16 years too (!), next are SMIL *and* MANIAC at 14 years.

Some are preserved: The IAS Computer, an IBM 701, part of BESK, JOHNNIAC, WEIZAC, part of SMIL, a FACOM 201 and TRASK (at least).

Family roots

The following is an outline of the IAS computer project from William Aspray's 1998 Paderborn Lecture *Von Neumann and the IAS Computer*

- 1945 John von Neumann decides he wants to build computer for scientific research
- persuades IAS to allow project, gets $100K
- RCA signs on to build memory device
- Army, Navy agree to pay most development costs - this machine to be a prototype for research, clones
- for military use
- later AEC and Air Force provide operating costs
- IAS reports distributed widely
  "On the Principles of Large-Scale Computing Machines" (1946),
  "Planning and Coding of Problems for an Electronic Computing Instrument" (3 Vol. 1947-48)
- construction completed 1952 (Selectron memory replaced by Williams tube)
- Research program in late 1940s and 1950s on Numerical Analysis ("internal economy")
- Research program in late 1940s and 1950s on scientific computing - meteorology, etc
- Opened way for daily numerical weather prediction
- 1956 machine sold to Princeton University
- 1957 project terminated.

The IAS Computer specification:

Technology	Around 3,000 vacuum tubes, with circuits interconnected by "3D" point-to-point wiring.
Operation	40 bit parallel operations with asynchronous arithmetic.
Arithmetic	Fixed point, twos complement sign and 39 bit fraction.
Instructions	16 instructions each with 16 variants. About 150 did something and of these some 20 covered most work. 20 bit, single address, 2 per word.
Memory	1024 words of 40 bits were provided by 40 Williams tubes.
Input and output	5 channel paper tape and printer, later additions included a magnetic drum and punched card input and output.

John von Neumann led the team which developed the IAS Computer. He did not patent the design as he was disgusted by legal proceedings between the US Government and the fledgling UNIVAC company over joint work at the Moore School on the EDVAC. The IAS Computer was a Government funded project and he was happy to provide circuits, progress reports, photos and advice to other research groups.

The family included Sweden's first electronic computer, Israel's first computer, Denmark's first computer, Australia's second computer, Japan's second computer and many firsts for the institutions involved. The "ancestral" IAS Computer was *not* the first member of the family to run!

| USA | ORDVAC | 1951 |

University of Illinois for the US Army
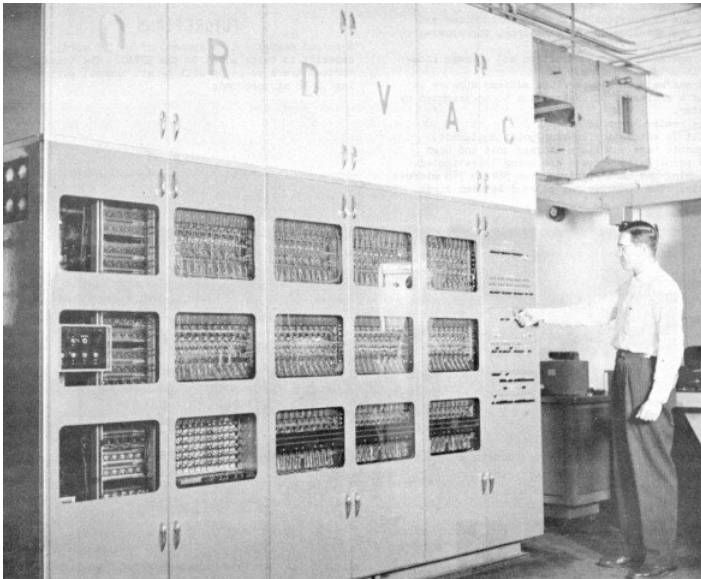
US Army photo

The *Ordinance Variable Automated Computer* was built at the University of Illinois for the US Army's Aberdeen Proving Ground. Construction began in 1949 under the direction of Ralph Meagher and with close support from the IAS group it was completed in November 1951, dismantled, shipped 600 miles (900 km) and rebuilt. ORDVAC was accepted in March 1952 at a cost of $250,000. It was used remotely from Illinois for 6 months. The team included Abe Taub, David Muller, Charles Williams and Jim Robertson along with software support from John Nash and David Wheeler (IEEE Computer Pioneer Award in 1985 "For assembly language programming") - visiting from Cambridge University.

It was used for weapon systems firing tables, design evaluation, war game problems etc.

Decommissioned: David Wheeler said "Well, the ORDVAC ... was probably one of the longest lived early computers, because I think it was still going 16 years later. Nobody knows actually when it died, which I find rather funny"   [Babbage Institute OH132]. Not Preserved.

Speed: Add time 42 usec, multiply 700 usec.   Average error-free running period 6 hours.
Construction: 3,430 vacuum tubes, 2,091 transistors, 915 diodes. Power 61 kw.
Modifications: card reader & punch, 1955: 10K word ERA drum memory, 1956: 4K core, 1958: floating point adder, 1961: index register, 1 inch magnetic tape. Alternative instruction set!   Added cost $350,000.

References: http://ed-thelen.org/comp-hist/BRL.html and BRL61.html,
  AFIPS Conference Proceedings 1985 National Computer Conference pp.31-37,
  http://ftp.arl.mil/~mike/comphist/   Thanks to Margaret Butler

USA	MANIAC	1952

Los Alamos National Laboratory

Photo Copyright © The Regents of the University of California

Paul Stein and Nicholas Metropolis

IEEE photo *

Nicholas Metropolis

MANIAC, the *Mathematical Analyzer Numerical Integrator and Computer* was built by the Los Alamos National Laboratory under the direction of Nicholas Metropolis and James Richardson. Metropolis is said to have chosen the name as a protest against the trend to make silly acronyms. The development team included Dick Merwin, Howard Parsons, Bud Demuth, Walter Orvedahl, and Ed Klein. Later software work was done by John Jackson and Mark Wells.

MANIAC ran from March 1952 at a construction cost around $250,000. It carried out the calculations for *Mike*, the first hydrogen bomb and ran applications for physical, mathematical, chemical, astronomical and biological research. The photo shows MANIAC playing *Anti-clerical chess* on a 6x6 board without bishops! LANL donated it to the University of New Mexico in 1957.

Decommissioned in 1966 after 14 years operation. Not preserved.

Speed: add 80 usec, multiply 1,000 usec
Construction 2,500 Vacuum tubes, 500 Crystal diodes. Power 35 Kw.
Memory: Williams Tube 1,024 words, magnetic drum 10K words.
Average error-free running period 5 Hours.

References: Proc.ACM Toronto 1952 pp.13-17,
   http://www.unm.edu/cirt/history.html
   http://lib-www.lanl.gov/la-pubs/00326886.pdf
   http://ed-thelen.org/comp-hist/BRL.html and BRL61.html

* J.A.N.Lee *Obituary of Nick Metropolis*, IEEE Annals of the History of Computing, January 2000, pp.86-87.

USA	IAS computer	1952

Institute for Advanced Study
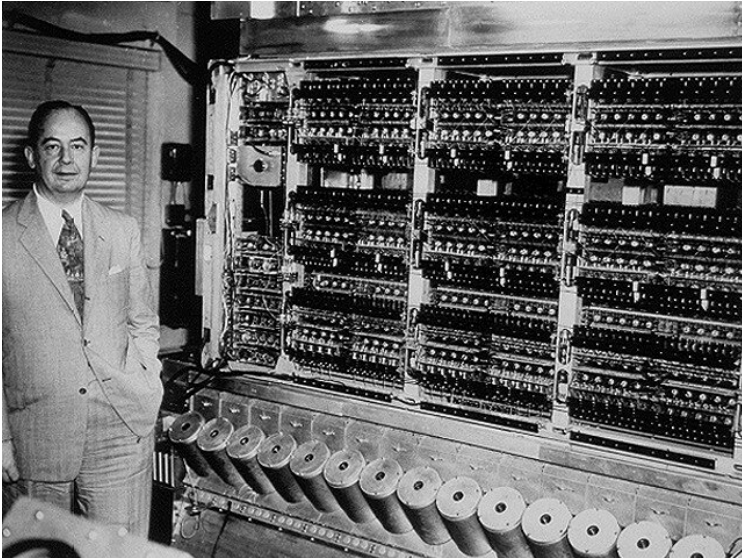
John von Neumann and IAS computer Photo by Alan Richards, courtesy of the IAS

The IAS computer was built at Institute for Advanced Study at Princeton NJ. It was developed by John von Neumann, Herman Goldstine, Julian Bigelow, Jim Pomerene (Computer Pioneer Award in 1986 "For IAS and Harvest computers"), Arthur Burks (Computer Pioneer award in 1982 "For his early work in electronic computer logic design"), Willis Ware (see JOHNNIAC), Gerald Estrin (see WEIZAC) etc. Development was outlined in the forward. This design was the model for *ALL* the machines described here. Completed in June 1952.

It was used for research in ballistics, aeronautics, hydrodynamics, elasticity, statistics, planning, physics & chemistry. The IAS closed its Computer Project in 1958 and presented the machine to Princeton University where it was for a while their prime computer.

Decommissioned in 1960 after 8 years operation. Preserved: In 1960 the IAS was donated to the Smithsonian National Museum for American History.

Speed: add 60 usec, multiply 700 usec.
Construction: 2300 valves. Power 16 Kw. Added: card reader and punch, 2K word drum.

References:

H.H.Goldstine *The computer from Pascal to von Neumann*
G.Estrin, *A description of the electronic computer at the Institute for Advanced Studies*,
    Proc.ACM Toronto 1952 pp.95-109
M.R.Williams *A History of Computing Technology*
G.A.Blaauw, F.P.Brooks, *Computer Architecture* (Addison-Wesley 1997)
http://ed-thelen.org/comp-hist/BRL.html

USA	ILLIAC	1952

University of Illinois

Photos courtesy of the University of Illinois

Ralph Meagher

The ILLIAC I *Illinois Automatic Computer* was built at University of Illinois in parallel with ORDVAC under the direction of Ralph Meagher. It became the first computer built and owned by a US educational institution in September 1952. Construction cost about $300,000. Much software was developed by David Wheeler from Cambridge University.

Major University users included: Agronomy, Educational Research, Chemistry, Electrical Engineering, Physics, Psychology and Structural Research. The "Illiac Suite" (as well as numerous minor musical items) were composed on this machine by a program developed by Lejaren Hiller and Leonard Isaacson.

Decommissioned: 1962 after 10 years operation. Not preserved:

Speed: add 40 usec, multiply 820 usec.
Construction: 2,800 vacuum tubes. Power 27 Kw.
Memory: Williams Tube 1,024 words.
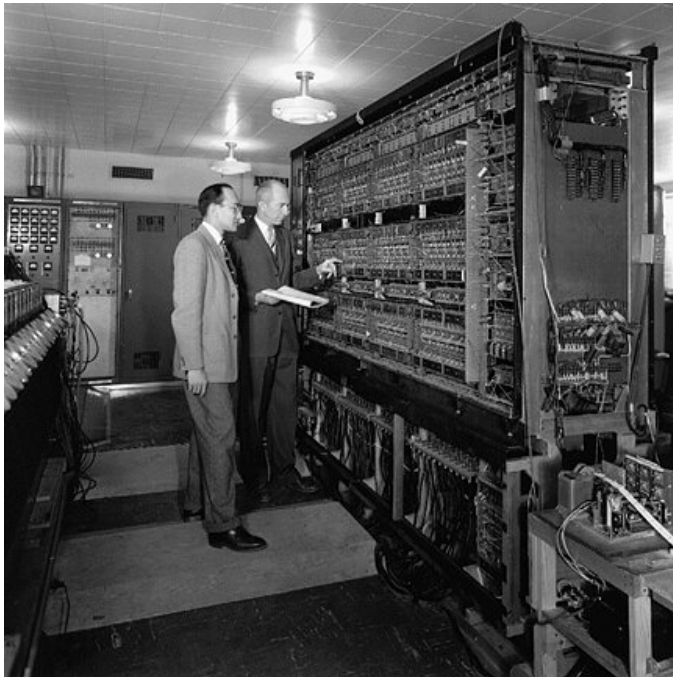Added: magnetic drum of 12K words, image device (256x256) and automatic camera.

References
  AFIPS Conference Proceedings 1985 National Computer Conference pp.45-50
  http://www.ieee.org/history_center/oral_histories/transcripts/ryder33.html
  http://www.cyberfest.uiuc.edu/achievementsparent.html
  http://ed-thelen.org/comp-hist/BRL.html and BRL61.html
  http://chem.pdx.edu/~wamserc/Hiller/6ILLIAC.htm

USA	AVIDAC	1953

Argonne National Lab

(Note the separate IAS style memory cabinet at the left)

Argonne National Lab photo

The *Argonne Version of the Institutes's Digital Automatic Computer* was built by Argonne National Lab. Construction was directed by Jeffrey Chuan Chu (Computer Pioneer award in 1981 "For his early work in electronic computer logic design") & Arthur Burks (of University of Michigan & IAS). Argonne staff included DA Flanders, J Alexander, D Jacobson, R Kramer, L Merrill. AVIDAC was completed 28 January 1953 and accepted in March. Its construction cost about $250,000.

AVIDAC was used for nuclear reactor engineering and related Atomic Energy Commission scientific and technical problem solving.

Decommissioned: late 1957 after 5 years operation. Not preserved.

Construction: 2500 tubes. Power from 355 batteries under generator charge.

References: http://www.anl.gov/OPA/frontiers96/comphist.html
  http://www.anl.gov/OPA/history/avidaccap.html
  AFIPS Conference Proceedings 1985 National Computer Conference pp.21-27,
  M.K.Butler, *Argonne National Lab*. in Encyc. Comp.Scie. & Tech. (Dekker 1975)
  Thanks to Margaret Butler.

USA	IBM 701	1953

IBM

Nathaniel Rochester

IBM's "Defense Calculator" was their first large-scale electronic computer, their first manufactured in quantity, their first scientific computer. It was a logical reworking of the IAS design with standard plug-in units and with 36 bit words. Company President Thomas J Watson Jr directed a large team under Nathaniel Rochester and Jerrier A. Haddad (Computer Pioneer Award in 1984 "For his part in the lead IBM 701 design team") which included M.M. Astrahan, J.W. Birkenstock, D.J. Crawford, P.E. Fox, W.W. McDowell, R.L. Palmer, R.D. Robins, H.D. Ross and *many* more. A system with magnetic tape rented for $17,500 per month in 1955, and were said to cost about $230,000.

John Backus developed "speedcode" for the 701 before designing FORTRAN.

19 systems were produced from April 1953 to April 1955, the later ones with core memory (of 4096 words). A cpu is preserved at IBM Somers.

Speed: add 60 usec, multiply 456 usec.
Construction: 4,000 valves, 12,800 diodes. Power 84 Kw.
Memory: Williams Tube of 2048 words of 36 bits each. Four drums, each 2048 words.
Four magnetic tapes (½ inch, 7 track). Page Printer, Card Reader and Card Punch (no paper tape), image display. Average error-free running period 5.4 hours.

References: http://ed-thelen.org/comp-hist/BRL.html and BRL61.html
  http://www-1.ibm.com/ibm/history/exhibits/701/701_intro.html
  J.W.Backus. *The IBM 701 speedcoding system*. J.ACM, 1/1, Jan 1954
  G.A.Blaauw, F.P.Brooks, *Computer Architecture* (Addison-Wesley 1997)
  Thanks to Peter Capek.
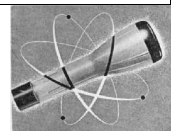
IBM 701 logo
(a memory tube)

Argonne National Lab for Oak Ridge National Lab
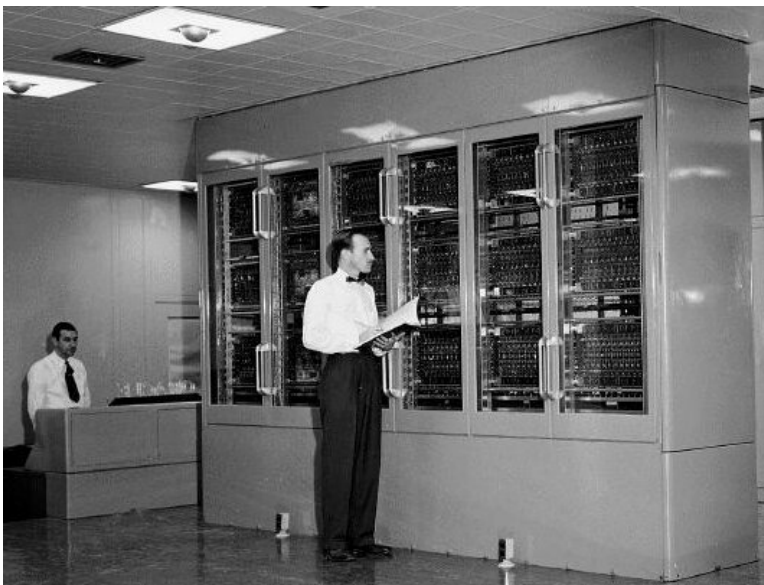
Oak Ridge National Lab photo

The *Oak Ridge Automatic Computer and Logical Engine* was built by Argonne National Labs for the Oak Ridge National Lab. Construction was directed by Jeffrey Chuan Chu & Arthur Burks after AVIDAC. ORACLE was completed in September 1953 & moved from Argonne to Oak Ridge where it was used from 4 February 1954. Oak Ridge staff included mathematician Alston Householder and engineers Earl Burdette, W. Gerhardt, Rudolph (Bud) Klein, Jerry Sullivan and Jim Woody.

Used for numerical analysis, programming techniques, and problems in physics, chemistry, engineering and biology. Decomissioned: late 1962 after 9 years operation. Not preserved.

Speed: add 70 usec, multiply 590 usec.
Construction: 5,000 valves, 200 diodes, 100 transistors. Power 75 Kw.
Memory: Williams Tube of 2,048 words unchecked or 1,024 words verified. Four magnetic tapes (2 inch, 42 track). Photographic plotter output.
Average error-free running time 4 hours.

References
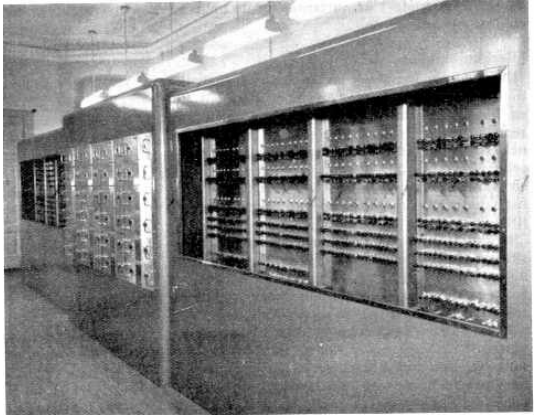 Proc.ACM Toronto 1952 pp.3-14 & 23-27 & 142-148
  http://ed-thelen.org/comp-hist/BRL61.html
  http://www.ornl.gov/ORNLReview/rev25-34/net425.html
  M.K.Butler, *Argonne National Lab*. in Encyc. Comp.Scie. & Tech. (Dekker 1975)
  http://ed-thelen.org/comp-hist/BRL.html
  Thanks to Margaret Butler & Bill Wing.

Sweden	BESK	1953

Royal Institute of Technology

| **Console and drum** | **BESK** | Photos courtesy of Jan Karlqvist at http://www.treinno.se/pers/okq |

The *Binär Electronisk Sekvens Kalkylator* (Binary Electronic Sequential Calculator) was built by the Swedish Royal Institute of Technology ("Matematikmaskinnämnden") at Drottninggatan in Stockholm for the Swedish Board for Computing Machinery. Following visits by Swedish scientists to Cambridge University and the USA in 1946, von Neumann lectured in Stockholm in 1949 and Erik Stemme joined the IAS project. Stemme returned in 1951 with IAS design details and Carl-Ivar Bergman extended the design to include floating point arithmetic. Olle Karlqvist (see EDB) built its magnetic drum and the team included Gösta Neovius and Hans Riesel all under the leadership of Stig Comét. BESK was completed in November 1953, Sweden's first electronic computer.

BESK was used for statistics, aircraft wing design for SAAB, engineering calculations for SKF, message decryption (the details are still secret) and some nuclear science work. Also the "Alphacode" assembler was developed.

Decommissioned in 1966 after 13 years operation. Only the operator's console is preserved at *Tekniska museet* Stockholm, Sweden.

Speed: add 56 usec, multiply 350 usec.
Construction: 2400 valves, 400 germanium diodes. Power 15 Kw.
Memory: 512 words of 40 bit Williams Tube memory and an 8K word drum (see page 36).

References: http://www.algonet.se/~rittsel/dator/besk1.htm
  http://www.scruznet.com/~luke/corres/riesel01.htm
  http://www.nada.kth.se/~riesel/
  http://www.treinno.se/pers/okq/index.htm
  Thanks to Par Rittsel, Martin Minow and Jan Karlqvist.

Carl-Ivar Bergman
Photo by Peer Ride
from Par Rittsel
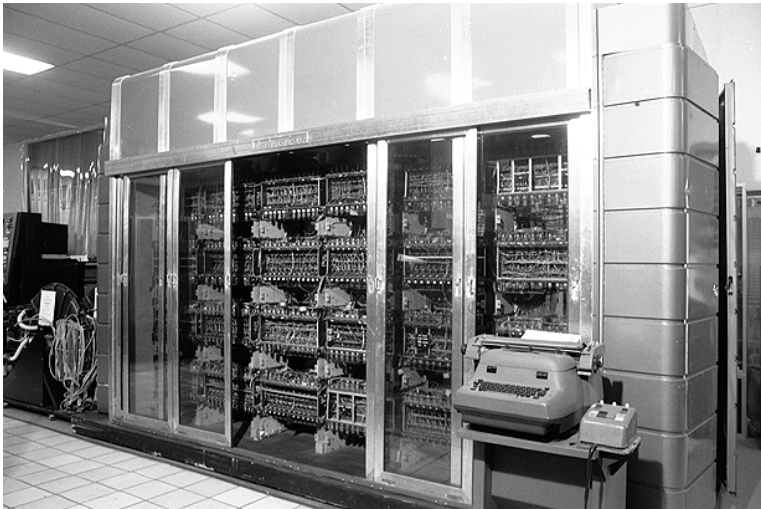
Rand Corp

Rand Corporation photo

The *Johnny Integrator and Automatic Computer* (an honour von Neumann was said not to have appreciated) was built by the Rand Corporation of Santa Monica. The project was directed by Willis Ware (Computer Society Pioneer Award in 1993 "For the design of IAS and Johnniac computers") who left IAS before that machine was completed. Bill Gunning was the Project Engineer and Mort Bernstein the software developer. RAND first built a *Johnniac Junior* 10 bit demonstrator. Johnniac was accepted in March 1954.

Used for scientific and engineering data processing problems. A transistor based adder was installed in 1957. Notable for the JOSS (*JOHNNIAC Open Shop System*) multi-user system and packet switching communications. Decommissioned in 1966 after 12 years operation and preserved in the Computer History Museum at Moffett Field, California.

Speed: add 25 usec, mult 400 usec. Later transistor add 0.8 us.
Construction: 5,000 valves, 500 crystal diodes, 1,400 transistors. Power 55 Kw.
Memory: 256 word RCA Selectron then from 1955 4K word magnetic core, 12K word magnetic drum. Card reader, card punch, printer, pen plotter. 1962: buffer interface for 10 IBM typewriters. Average error-free period 10 hours.
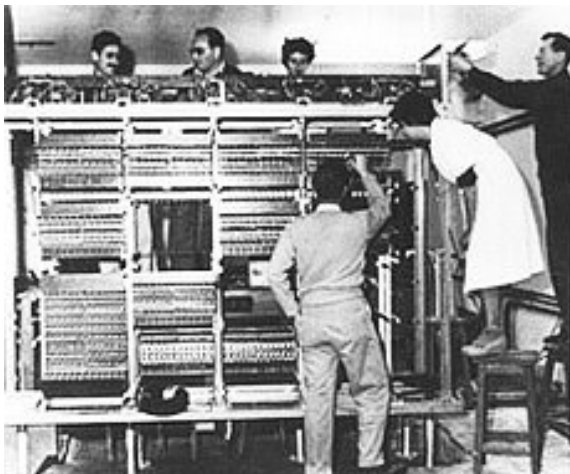

Willis Ware IEEE photo

References:
  Fred Gruenberger *History of the JOHNNIAC* (Rand)
  J C Shaw *JOSS* AFIPS Fall 1964 pp.455-464.

 http://www.computerhistory.org/events/johnniac_09151998/ johnniac_xscript.html
 http://ed-thelen.org/comp-hist/BRL.html and BRL61.html
 Thanks to Willis Ware.

Israel	**WEIZAC**	**1955**

Weizmann Institute

Weizmann Institute photo   **Gerald Estrin** IAS photo

The *Weizmann Automatic Computer* was built at the Applied Mathematics Department of the Weizmann Institute of Science, Rehovot Israel. Construction was initiated by Chaim Pekeris and directed by Gerald Estrin (IEEE Computer Pioneer Award in 1995 "For significant developments on early computers") who worked on the IAS. His team included Thelma Estrin, Ephraim Frei, Micha Kedem, and Zvi Riesel. Based on the IAS design, WEIZAC, Israel's first computer, ran in October 1955.

WEIZAC was intensely used for physical problems including modelling ocean tides, helium atom analysis, earthquake data processing, and training.

Decommissioned: 29 December 1963 after 8 years operation. Preserved at the Ziskind building at the Weizmann Institute.

Speed: add 50 usec, multiply 750 usec.
Construction: initial drum memory, 4K word magnetic core memory from October 1956. Magtape from 1958.

References:
http://wis-wander.weizmann.ac.il/weizmann/doa_iis.dll/Serve/item/English/1.101.4.9.2.html
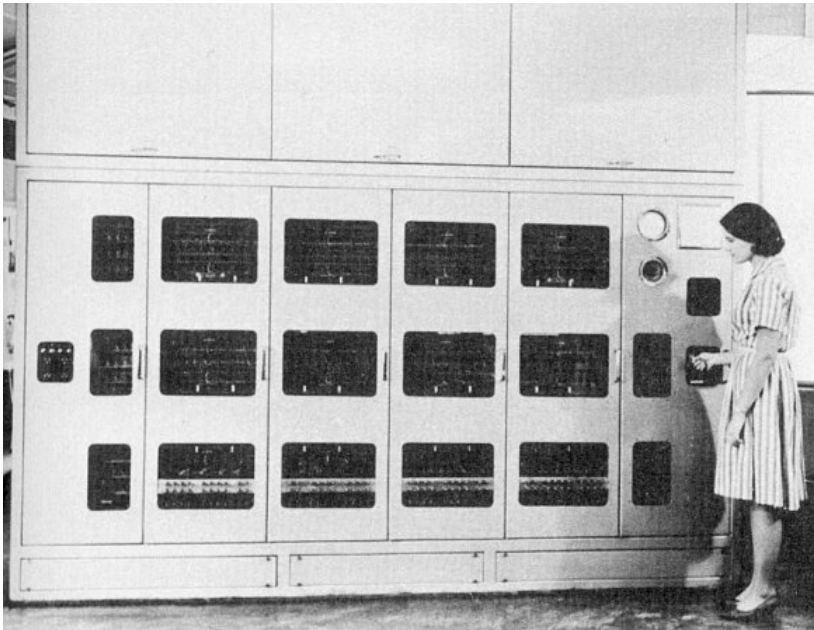http://wis-wander.weizmann.ac.il/weizmann/doa_iis.dll/Serve/item/English/1.101.3.2.8.19.html
Gerald Estrin *The WEIZAC Years (1954-1963)* Annals of the History of Computing October-December 1991 (Vol. 13, No. 4) pp. 317-339.

Australia	**SILLIAC**	**1956**

University of Sydney

Pat Dunlop operating SILLIAC

Photos courtesy of the Uni. of Sydney Science Foundation for Physics

Sydney's ILLIAC was built at the University of Sydney, Australia. A copy of ILLIAC I, construction was directed by Brian Swire whose team included Barry de Ferranti and Peter Aplin with software by John Bennett. SILLIAC was completed in June 1956.

SILLIAC was used by Australian and NZ computer departments, government and industry for projects ranging from helium physics, cosmic ray air shower analysis and X-ray diffraction data processing to aircraft design, hydro-electric planning and payrolls. It was used for teaching and development of an early local area network.

Decommissioned: May 1968 after 12 years operation. Not preserved.

Speed: add 73 usec, multiply 720 usec.
Construction: 2800 valves. Power 35 Kw.
Four bidirectional magnetic tape units.
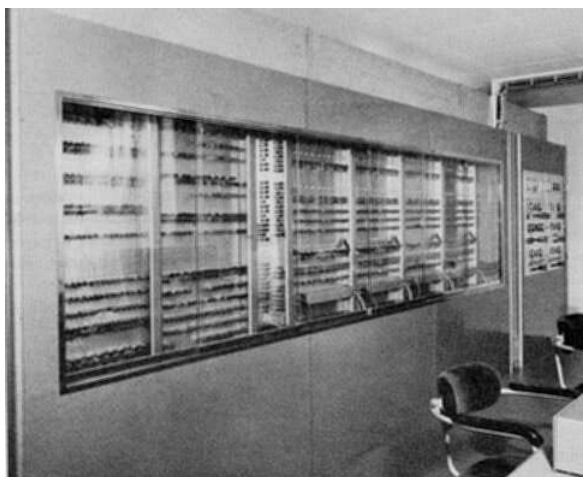Average time between faults about 6 hours.

References: Thanks to John Bennett, Barry de Ferranti.
  Incidentally, John Deane, *SILLIAC - vacuum tube supercomputer* (ACMS in preparation).

Brian Swire

Sweden	**SMIL**	**1956**

Lund University

Photos courtesy of Lund University

Operating console

SifferMaskinen I Lund (Lund Digital Machine) or "smile" was built at Lund University in Sweden. It was a simpler version of BESK which used magnetic drum memory & was completed in June 1956. It was developed by Professor Carl-Erik Fröberg. Much of the construction, and subsequent maintenance was carried out by Kjell Jönsson.

Decommissioned: 1970 After 14 years operation. Preserved: (partly) at the Malmö Technical Museum in Stockholm.

Construction: 2,000 tubes 200 germanium diodes, Power 12 Kw.
Memory: originally 2K word drum memory, expanded to 4K then replaced by magnetic core.
Additions: magtape carousel (total 512 K words, see EDB-1), punched cards, line printer. And a floating point maths unit.
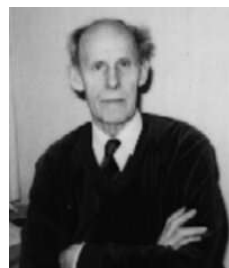
References:
Fröberg, Carl-Erik, and Wahlström, Gunnar: "*SMIL. Siffermaskinen i Lund"*. (Acta Regia Societatis Physiographicae Lundensis. Vol.68, p.38, 1957.)
Lysegård, Anna "*Programmering för SMIL*" (1966–Ur)
http://www.mai.liu.se/BIT/history.html
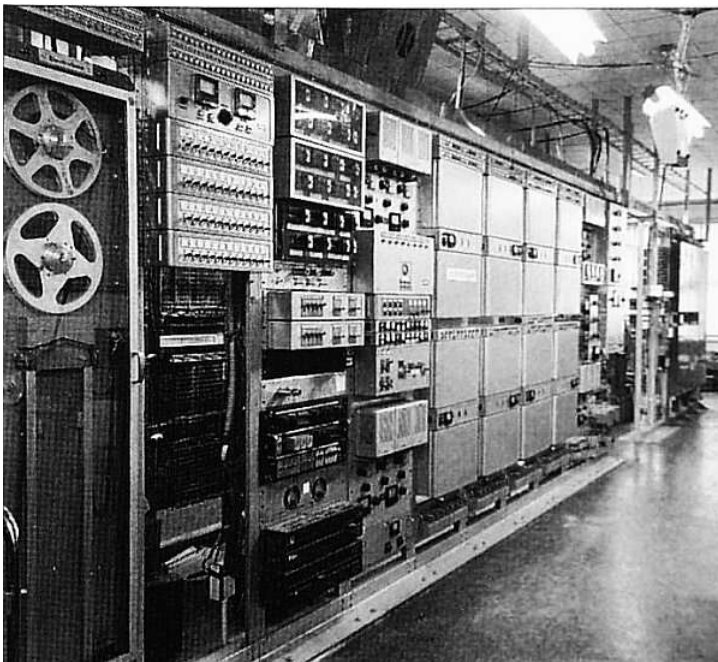Thanks to Par Rittsel, Lars Gislén and Bo Thoren of Lund University Library.

Carl-Erik Fröberg
Lund University photo

NTT

NTT photo

MUSASINO-1 was named after the Musasino district near Tokyo where it was built by Nippon Telegraph and Telephone Corp. It was based on the IAS computer but used different technology. It was completed in March 1957 - Japan's second computer.

Decommissioned: July 1962 after 5 years operation. Not preserved.

Speed: add 480 usec, multiply 5 msec.
Construction: 5,400 parametrons - logical elements based on ferric inductors and phase difference rather than voltage level - invented by Eiji Goto in 1954. Also used 519 valves. Memory 32 word drum, extended to 256 word drum.

References:
> http://www.comp.ae.keio.ac.jp/pub/simulator/
> Satosi Endou, "*Keisankiya kaku tatakaeri*" (Japanese computer pioneers thus struggled) in Japanese (ASCII of Japan 1996).
> Thanks to Seiichi Okoma, Keio University.

Eiji Goto
Tokyo University photo

17

Facit

EDB* with Olle Karlqvist   Photo from the "Karlqvist family album" at http://www.treinno.se/pers/okq

A version of BESK (without floating point) built by Åtvidabergs Ind. (known as Facit) at Karlavägen under the direction of Olle Karlqvist, who had worked on BESK. He described it as a "cautious first copy". It was used from 1957 as a service bureau.

Decommissioned: about 1962 after about 6 years operation. Preserved: ?

Construction: valve technology with 2K words of core memory.

Reference
  Proc.IRE Jan 1961,
  http://www.algonet.se/~rittsel
  http://www.treinno.se/pers/okq/index.htm
  Thanks to Par Rittsel and Jan Karlqvist.

The Facit *ECM-64* "carousel" tape drive was developed by Erik Stemme (see BESK) and used on the EDB series and on many Scandinavian computers. Removable "wheels" carried 64 magnetic tape spools each with a capacity of 8K words.

Photo courtesy of the Facit-archive i Atvidaberg

* This photo is not EDB-1. It was taken at the 1966 party at Facit in Solna to farewell Olle Karlqvist.

Facit

**The operator's console
and paper tape equipment**

Photos courtesy of G.Holmdahl

The system installed at ASEA

Commercial versions of BESK (via EDB-1) were also made by Åtvidabergs Industries (or Facit) from 1957 using vacuum tube and transistor technology with core or drum memory. At least 8 were produced including systems for Facit Stockholm in 1957, ASEA at Västerås (Sweden) in 1958, Facit Göteborg (Sweden) in 1960, Original Odhner in 1961, Facit Solna in 1962 and Facit Dusseldorf (Germany) in 1963.

ASEA (now ABB) is a large Swedish electrical equipment manufacturer. Their EDB installation cost about 1.5 m kronor and was used for technical and scientific applications until 1966 (when it was replaced with a GE 625 system).

Decommissioned: ASEA: 1966 after 9 years operation, not preserved. *And the other 7?*

Speed: add 45 usec, multiply 290 usec.
EDB2: core memory 2K to 64K words (!), paper tape.
EDB3: 8K word drum memory, card reader and punch.
(but the ASEA machine had 2K core and a 4K drum) Power 20 Kw, weight 2000 kg.
Both had a "carousel" tape unit able to house 64 reels (see EDB-1).

References:
  Proc.IRE Jan 1961,
  http://www.algonet.se/~rittsel
  Thanks to Par Rittsel, Gunnar Holmdahl, Roy Andersson of *Facit-archive i Atvidaberg*.

Sweden	SARA	1957

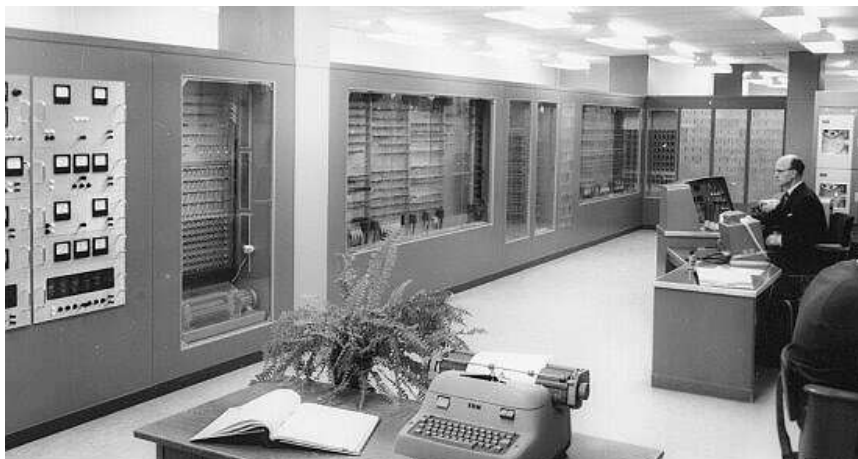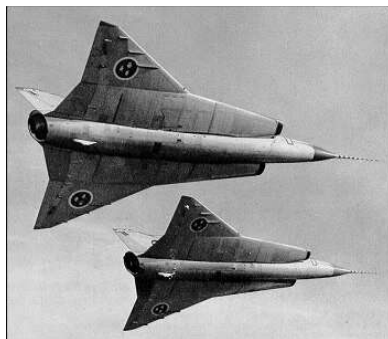**SAAB**

Saab's aritmetiska Räkneautomat (ie Saab's automatic calculating machine) was built following Saab's purchase of the design of BESK in 1955. The improved design was not compatible with BESK. SARA was completed in 1957 under the direction of Börje Langefors head of their department for numerical analysis, and later professor at the University of Stockholm (AIS LEO Award for Lifetime Exceptional Achievement in Information Systems 1999). One of the hardware engineers was Bo Ragnemalm and Bengt Asker worked on the software.

SARA was built to carry out design calculations for the jet fighter *Draken.*

Decommissioned in 1967 after 10 years operation. Not preserved.

Speed: add 56 usec, multiply (and divide) 364 usec.
Construction: vacuum tubes, 40 bit words, 20 bit instr (12 bits address and 8 bits operation). Core memory of 2048 words, paper tape input and output, an 8K drum and six ¾" magtapes.

**SAAB Draken** SAAB photo

References: IEEE Trans.Electronic Computers, Dec 1963, p.651,
   http://www.algonet.se/~rittsel ,   http://www.aisnet.org/award/leorecip.shtml#langefors
   http://www2.ctrl-c.liu.se/misc/datasaab/om-eng.html
   Thanks to Julie McCurry, Bengt Asker, Bo Ragnemalm and Curt Murhed of the Saab Veterans Club (http://www.saabsveteranklubb.nu). This has about 30,000 photos from all Saab products and facilities including many of SARA.

Denmark	**DASK**	**1957**

Academy of Technical Sciences
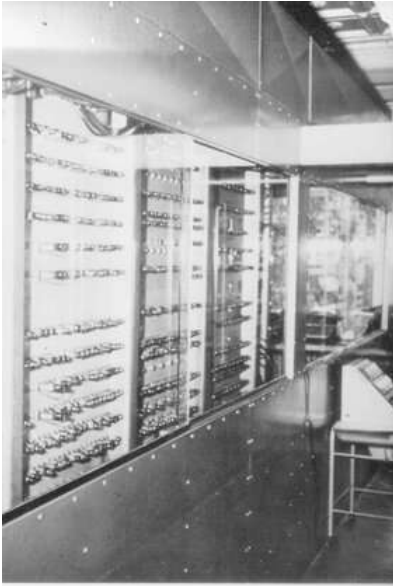
Bent Scharøe Petersen

Danish Datahistory Museum photos

The *Dansk version of BESK* (a more technical acronym was made later) was a version of Besk built by the Danish *Akademiet for de Tekniske Videnskaber* (Academy of Technical Sciences) under the direction of Bent Scharøe Petersen. DASK was constructed in Copenhagen's Valby district, near the Carlsberg brewery. It had advanced features such as an index register and provision for remote operation and it was completed 29 September 1957 - the first computer in Denmark. Construction cost around US$140,000.

DASK was used for programming classes by the *Danmarks Tekniske Højskole* (now Denmark's Technical University) and for nuclear sciences research.

Decommissioned in 1960 after 4 years operation. Preserved: ?

The core memory was "sewn" together by the wives of staff members. It had a drum, line printer, punched cards and magtape.

References:
http://www.beagle-ears.com/lars/engineer/comphist/dan_hist.htm
http://www.datamuseum.dk/site_dk/rc/dask/
Per V.Klüver, *From Research Institute to Computer Company: Regnecentralen 1946-1964,* IEEE Annals of the History of Computing April-June 1999 (Vol. 21, No. 2) pp. 31-43.
Thanks to Par Rittsel.

USA	MISTIC	1957

Michigan State University

"Butch" Henderson operating MISTIC   Michigan State University photo

The *Michigan State Integrated Computer* was constructed under the direction of Dr. Lawrence W. VonTersch (*see back cover*).The team included Richard Reid, Julian Kateley, M. Glen Keeney and Jerry Weeg. John Ryder wrote "At Michigan State, we copied the ILLIAC and called it the 'MISTIC'. I invented the name, Michigan State Integrated Computer or something like that. We copied it and Illinois told us it would cost $120,000 to build it." It was completed in November 1957.

MISTIC provided a computing facility for University staff and students and it was used for many programming and numerical analysis courses. A major user was New Zealander Charles Wrigley who made major contributions to statistics.

Decommissioned: late 1963 or 1964 after 7 years operation. Not preserved.

Construction: 2610 valves. Power 19 Kw.
Used Hollerith cards and paper tape for input. Later 16K core memory was added.

References
  http://www.ieee.org/history_center/oral_histories/transcripts/ryder33.html
  http://www.cse.msu.edu/NewsLetters/Fall98/F98PROC4.htm
  http://ed-thelen.org/comp-hist/BRL61.html
  Many thanks to Glen Keeney.

Iowa State University

Iowa State University photo by Richard Horton

CYCLONE (an arbitrary name indicating high speed) was built at Iowa State University. It was a copy of ILLIAC constructed under the direction of Robert Stewart and Ralph Schauer with a team which included Roy Zingg. Completed July 1959. Art Pohm designed the 16K core memory which replaced the original Williams-tube memory.

Used for general purpose computing to support research work on campus.

Decommissioned: "mid 1960s" after about 6 years operation. Not preserved:

Speed: add 70 usec, multiply 960 usec.
Construction: 2571 valves. Initial 1K words of Williams tube memory was replaced with 16K of core. Power 19 Kw.

References
  "Green Hills" (ISU press, 1975)
  http://ed-thelen.org/comp-hist/BRL61.html
  http://www3.ee.iastate.edu/pop/History%20of%20ECPE/1950s/Cyclone%20Lab.html
  Thanks to Glen Keeney, Terry Smay and Jim Triska.

Japan	FACOM 201	1960

Fujitsu
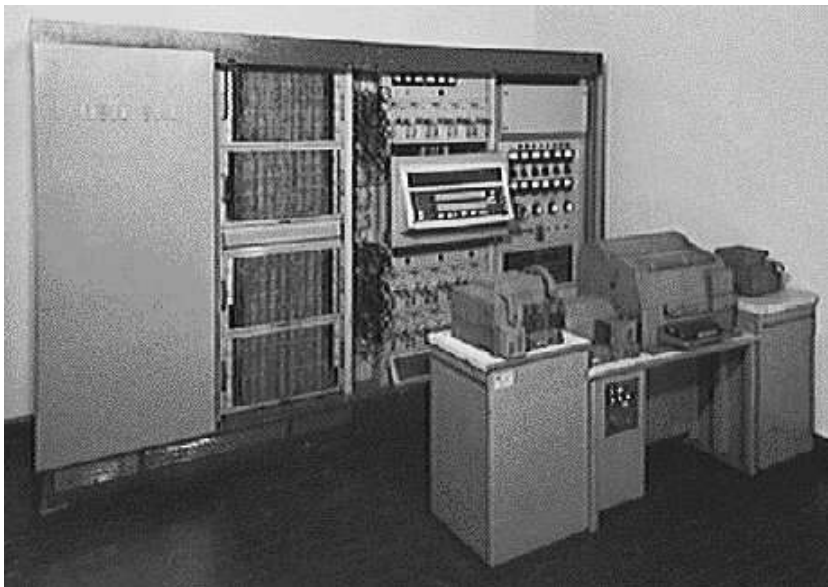
NTT completed Musasino-1 in 1957 and Fujitsu was asked to commercialise the machine. Fujitsu produced the FACOM 201 using exactly the same board layout. Fujitsu delivered No. 1 (aka Musasino-1B) to NTT's *Denki Tsuushinn Kenkyusho* (Telecommunication Laboratory) in March 1960.

No. 2 with improved, lower current, parametrons was delivered to *Tokyo Rika Daigaku* (the Science University of Tokyo) in May 1960.

Decommissioned: when? One is preserved at the Science University of Tokyo, Science and Technology Museum.

Speed: add 2 msec, multiply 35 msec.
Construction: 5,500 parametrons (phase based logic element driven at 2 MHz, invented by Eiichi Goto). 1024 words of magnetic core memory.

References:
  http://www.sut.ac.jp/edocs/faci/museum.html
  http://www.fujitsu.co.jp/people/kanda/comp/old
  Thanks to Naoimi Hoida of Fujitsu, Seiichi Okoma of Keio University, Yasunori Kanda of Fujitsu, and Hajime Suzuki for translations.

Sweden	TRASK	1965

Datasystem AB

Photo from Thomas Lindblad

In 1959 Datasystem AB was formed by Axel Bring, Gunnar Hellström and Zoltan Horvath to build a "Super BESK" for the Swedish Government - but the Government decided to purchase an IBM 7090 instead. Eventually this version of BESK was built for *The Nobel Institute of Physics* (later *The Research Institute of Physics*). TRASK *"TRAnsistorised Sequential Calculator"* was completed in August 1965.

TRASK was very reliable and was run for an average of 200 hours every month. It was used primarily for Institute research and became available for outside work including calculations for the mining industry and for construction of the Lidingö Bridge in Stockholm.

Decomissioned in 1980 after 15 years operation. Preserved at the *Tekniska museet* in Stockholm, Sweden.

Construction: encapsulated transistor circuit packages, core memory. BESK compatible. A Facit 64 spool "carousel" magtape was added.   (see EDB-1, also see p.40)

References: http://www.telemuseum.se/utstall/transistor/trask.html
  http://w1.876.telia.com/~u87624751/trask.pdf   (by Thomas Lindblad)
  http://www.algonet.se/~rittsel
  http://www.merrymeet.com/minow/
  Thanks to Martin Minow, Eva Derlow of the Telemuseum Stockholm, Matts Ramberg curator at the *Tekniska museet* and Asa Jamting for translations.

Distant family members

The following projects have some link to the IAS computer family, but they are <u>not</u> copies.

Netherlands	ARRA II	1953

Mathematical Centre

Photo courtesy of the Centrum voor Wiskunde en Informatica, Amsterdam

The *Automatische Relais Rekenmachine Amsterdam II* (Automatic Relay Computer - ARRA I *was* a relay computer) was constructed at the *AmsterdamMathematisch Centrum* (Amsterdam Mathematical Centre - now *Centrum voor Wiskunde en Informatica* - Centre for Mathematics and Computer Science). The team was led by Dr. G.A. Blaauw who identified the design as based on the IAS *and* Harvard Mk IV. However, the architecture is serial using magnetostrictive delay lines and it is physically distinct.

Construction: vacuum tubes, selenium diodes mounted on flat plug-in units.
Memory: three fast memories of magnetic delay lines, 1024 word drum.

References:
   http://www.cwi.nl/cwi/about/history.html
   http://www.digidome.nl/gerrit_a__blaauw.htm
   G.A.Blaauw, F.P.Brooks, *Computer Architecture* (Addison-Wesley 1997)

Netherlands	FERTA	1954

Mathematical Centre for Fokker

Fokker Electronic Calculating Machine Type ARRA was an improved copy of ARRA II built in 1954 and installed at Fokker.

USA	MANIAC II	1956

Los Alamos National Laboratory
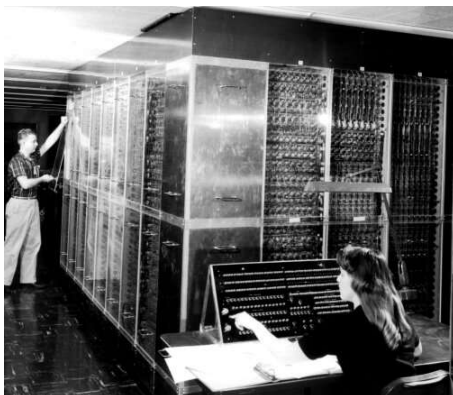
Based on MANIAC I but with changed architecture. MANIAC II included floating-point arithmetic and indexed addressing.

Used to 1977.

Construction: 5,190 tubes, 3,050 diodes, 1,160 transistors.
Memory: 48 bit words, 12K words of electrostatic memory and 4K core, three magtape units (using $^1/_4$" tape)

Reference
http://ed-thelen.org/comp-hist/BRL61.html

LANL photo

USA	GEORGE	1957

Argonne National Lab

The design was based on experience gained from the two earlier machines constructed there (AVIDAC and ORACLE). Construction was directed by Jeffrey Chan Chu, Jean Hall and Herb Gray, completed September 1957.

Used for scientific problems, data handling and data reduction. Closed down 11 April 1966.

ANL photo

Construction: vacuum tube technology and core memory. A transistor floating point unit was added. 3,500 tubes, 6,000 diodes, 20,000 transistors. Power 50 Kw.
Memory: 4K core of 40 bit words. Variable length instructions 20 to 100 bits. Four magtape units using 2" tape.

Reference
AFIPS Conference Proceedings 1985 National Computer Conference pp.21-27
http://ed-thelen.org/comp-hist/BRL61.html
Thanks to Margaret Butler.

USA	Rice Institute Computer / Rice University Computer / R1	1959

Rice University

This was somewhat based on the Los Alamos National Labs MANIAC II, so it is a 3rd generation of the IAS family. It had and a "tagged architecture" to support virtual memory. Partially operating in 1959 it was used from 1961 to 1971.

Martin Graham designed the hardware of the Rice Computer, and most of his plans were implemented by Joe Bighorse, the project's head technician. Construction on the machine proceeded from 1958-1961. A copy of the machine was also built at the University of Oklahoma.

Construction: vacuum tube, electrostatic memory with 56 bit words and one instruction per word with indirect addressing. "The architecture of the Burroughs B5000 closely resembles the Rice Computer"
Line printer, two magnetic tape units (later four), limited disk subsystem.

Reference www.cs.rice.edu/History/R1

USA	MERLIN	c.1959

Brookhaven National Lab

MERLIN was built by Brookhaven National Lab. It was based on the MANIAC II with augmented memory and floating point arithmetic. It was completed by 1960 under the direction of Dr Bob Spinrad and Marty Graham.

Used for Atomic Energy Commission programs, including physics, chemistry, biology, medicine, reactor studies, accelerator design etc. It collected real-time parallel data via 48 coax cables from BNL's particle accelerator "half a mile away". Later, one inch magnetic tape drives were added. Decomissioned: around 1968.

Construction: 1075 valves, 7000 diodes, 800 transistors. Power 40 Kw.
Memory: electrostatic store using RCA tubes: 4096 words of 48 bits with 5 bits for single bit error correction & duplicated for redundant error correction. Could operate as 8192 words of less reliable memory. Two bits were available for software tags.
Time between failures "was, at best, about an hour".

References:
  http://www.ccd.bnl.gov/LINK.bnl/1995/Nov95/histcom1.html
  http://ed-thelen.org/comp-hist/BRL61.html
  Thanks to Ray Borrill.

Adopted family members

These machines have been described as members of the IAS computer family, but I believe they are <u>not</u>.

USSR	BESM 1	1952

Institute for Precise Mechanics & Computer Engineering
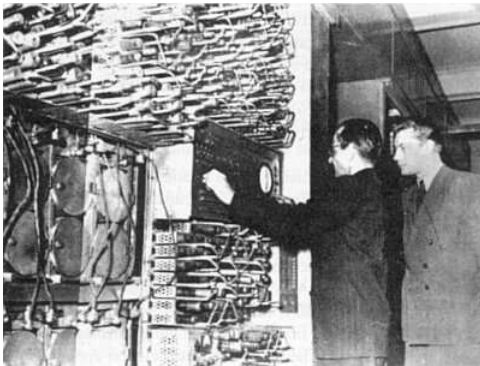
BESM-1 with Sergei Lebedev and A.A.Sokolov
Russian Computer Museum photo

Bystrodeistwujuschtschaja Elektronnajastschethaja Machina (Big Electronic Computing Machine) was built at the *Institute for Precise Mechanics & Computer Engineering*, Academy of Sciences of the Soviet Union in Moscow. Developed under the direction of Sergei A. Lebedev (IEEE Computer Pioneer Award in 1996 "For the first computer in the Soviet Union"). Lebedev developed Russia's first computer MESM and went on to develop a long line of successful computers (BESM-6 was particularly significant). BESM-1 was completed in 1952.

The Swedes have no doubt about the design origins - Par Ritsel wrote
> It has always been said that the blueprints for Besk ended up in Moscow. No one has ever told me how. But the Besm is considered by all veterans as a sister machine to Besk.

Professor Carl-Erik Fröberg (who built SMIL, the smaller Besk copy in Lund):
> It should be mentioned, that the first Russian machine BESM quite obviously borrowed a lot of features from BESK.

(Fröberg, *Datamaskiner*, Gleerups, Lund 1965)

Lebedev and his colleagues read western journals and received copies of von Neumann's major reports (as did research institutes all round the world) so there was influence - but neither the architecture nor the implementation seem to me to show a close resemblance to IAS machines.

Construction: 4000 tubes.
Memory: 1023 words (yes, address 0 was a permanent 0 word) of 39 bit Williams Tube memory (later replaced by magnetic core). Plus 1K of diode ROM memory.
One 3 address instruction per word, floating point.
Four magtapes (1/4"), 5K word drum, fast photo printer.

References
  IEEE Annals of the History of Computing 21/3 October 1999

http://www.icfcst.kiev.ua/museum/Lebedev.htm

http://www.computer-museum.ru

Peter Wolcott, Seymour E. Goodman: High-Speed Computers of the Soviet Union. IEEE
Computer 21(9): 32-41 (1988)

Boris N. Malinovsky "Soviet computer pioneers", Kyiv, 1995

Thanks to Par Ritsel, Sergei Prokorov, Professor Alexandr Tomilin.

Germany	PERM	1955

Technische Hochschule

PERM   Deutsches Museum photo

Programmgesteurte Elektronische Rechenanlage München (Program-Controlled Electronic Computer Munich) was built at the Technische Hochschule Munich Germany. Developed by Hans Piloty and mathematician Robert Sauer with a team including Friedrich L Bauer (who designed the floating point arithmetic unit, IEEE Computer Pioneer Award in 1988 "For computer stacks"), Klaus Samelson, Heinz Schecher & Alfons Gottwald. Completed in 1955.

Decommissioned in 1974 after 19 years use. Preserved in the *Deutsches Museum* Munich.

PERM is described as having been guided by the IAS design, but it had floating point arithmetic, 50 bit words, a very large instruction set and complex addressing modes. The physical construction is also separate.

Construction: Tube logic.
Memory: 50 bit core memory, 8K word drum
16 bit order code + 2 bits address type: direct, modified or indirect. 3 floating point formats.

Reference
Comm ACM 4/6 June 1961 Blachman pp.256..265

http://wwwbib.informatik.tu-muenchen.de/Stroehlein/Fak_Schrift_97/engl.Version/IN_Zeit_2_eng.html

http://www.deutsches-museum.de

http://wwwbib.informatik.tu-muenchen.de

Thanks to Heiner Besthorn, Peter Krauss and Winfried Hahn.

Kidnapped family members

Some machines have been described as family members for no good reason that I can see.

UK	EDSAC	1949

Cambridge University

Maurice Wilkes' famous contender for the first usable computer. This is a serial machine explicitly based on the von Neumann/Moore School EDVAC design.

Australia	CSIRAC	1951

CSIRO Australia
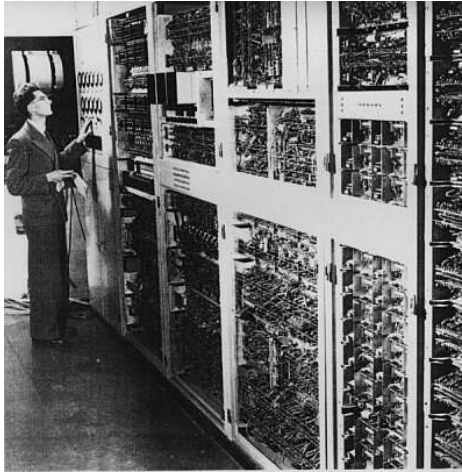
A pioneering effort by Trevor Pearcey (shown here with CSIRAC) and Maston Beard. A serial, 20 bit machine with an unusual approach to instructions. Probably influenced by the EDVAC design, but not following it.

CSIRO Australia photo

USA	Whirlwind	1951

MIT

Herman Goldstine believed this was based on the IAS because Jay Forrester received copies of all the IAS design and circuitry. This may be so at a very low level, but architecture and physical construction are quite distinct.

"USA"	TC1	"1953"

International Telemeter Corp

Mentioned by Emerson Pugh in "Memories that shaped an industry" in a letter attempting to get a better price from IBM for core memory products - there is no reason to think it was ever built. ("TC-1" was also a version of the IBM 360 used later in Skylab)

Building The Beast

There should be wonderful collections of photos of building the IAS computer and ILLIAC. Willis Ware took the photos of the IAS machine for others to use and Michigan State received a massive set from the University of Illinois. As far as I know these have not surfaced yet. While all the machines were different it seems fair to mix-and-match photos as many were very similar and all met very similar specifications.

First you needed circuit drawings from your good friends at the IAS / University of Illinois / etc. (photo at STC for SILLIAC)

You started with a metal frame. (SILLIAC)

University of Sydney photos

Someone started building the tube based electronics:
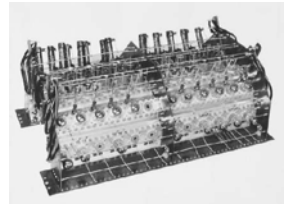
(STC for SILLIAC)

and these were inserted in the frame. (MISTIC with Lawrence VonTersch)
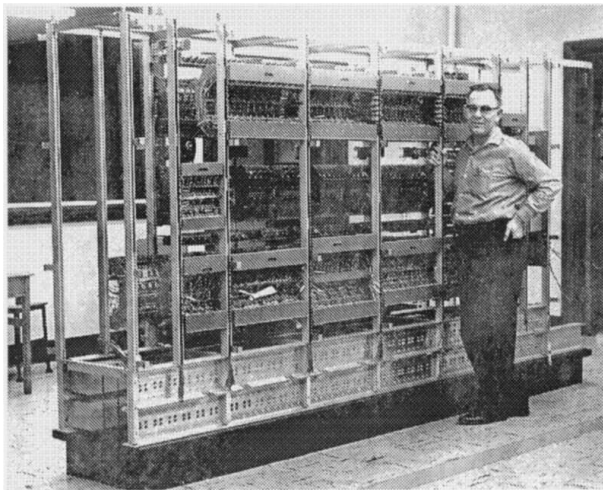
Michigan State University photo

University of Sydney photo

Someone had to solder all the chassis interconnections. (Barry de Ferranti left & SILLIAC)
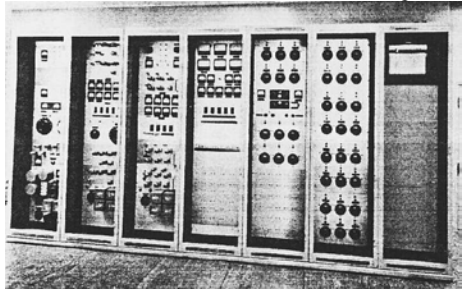
Soon you would want to start testing parts of The Beast. You needed power supplies – lots of them - with enough capacity for a small town and flexibility to vary each voltage for testing. (ORACLE power supply)
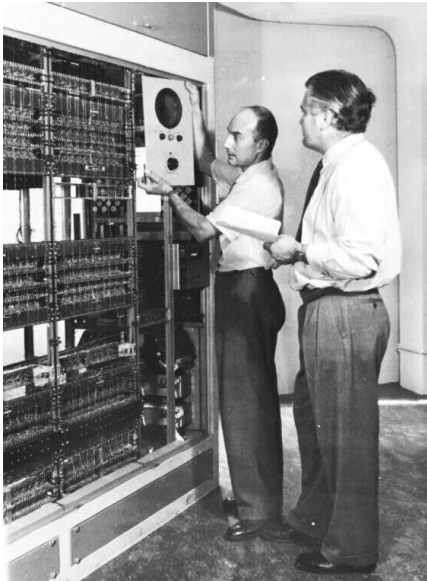
University of Sydney photo

There was a slave display tube to install. (Fred Gale, Brian Swire & SILLIAC)

And a lot of chassis to put in. (Ralph Schauer and Robert M. Stewart with CYCLONE)
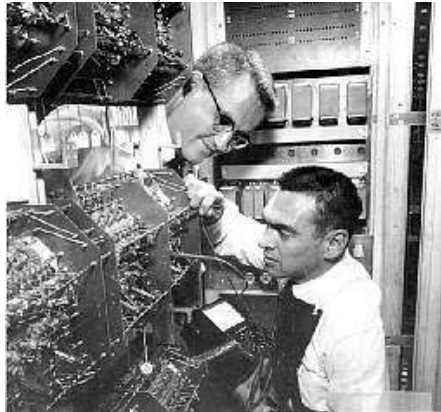
Iowa State Uni photo by Richard Horton

The memory was always a big deal – with ORACLE you didn't need to climb a ladder! (Margaret Butler & Bud Klein   ORNL photo)
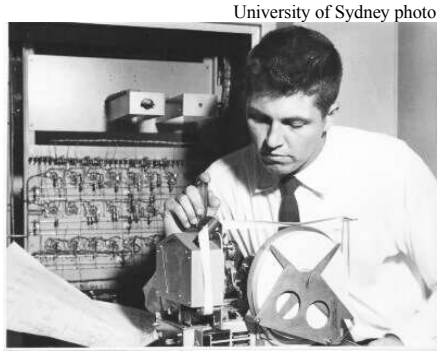
Everything down to the paper tape punch had to be checked and adjusted. (Barry de Ferranti, SILLIAC)
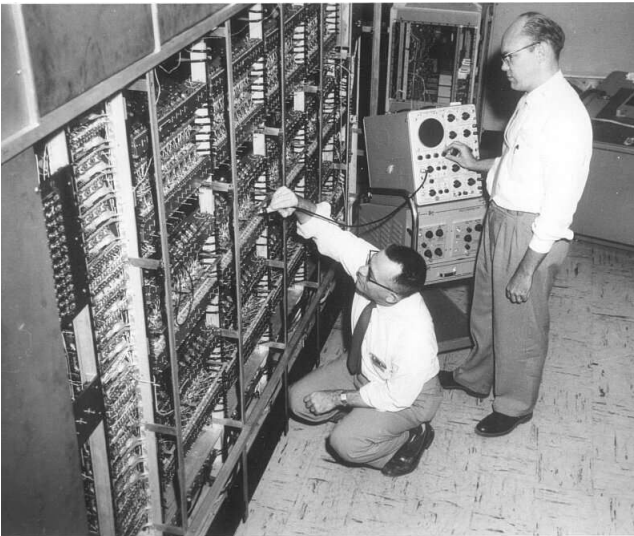
Of course you never finished. These Beasts had a mean time between failures a little less than a working day (or 8 hour shift in most cases). Circuit detectives and solder jockeys were needed all the time.

(Lawrence VonTersch and Glen Keeney with MISTIC)

The finished hand crafted computers can be seen all through this book!

The technology

1. Vacuum tube / thermionic valve logic

These were (almost) the only practical electronic logic device available until reliable transistors were produced in the early 1960s.

A triode consisted of a central filament heated to a red hot glow by a low AC voltage. This is where most of the current was consumed. This heated the "cathode" metal plate to provide a source of electrons. With a substantial voltage (say 300 V DC) between cathode and "anode" plate a current could flow. The amount of current depended on the voltage on the open grid of wires between them. This all had to happen in a vacuum enclosed by a glass envelope. Many IAS class machines used minature twin triodes as illustrated (2C51 for SILLIAC).

This structure was fragile, the filament had a finite lifetime and the glass-metal joint where the wires entered would eventually leak air. Even with an expected tube lifetime of 1000 hours, failure of one of the ~3000 tubes was the principal operational problem.

2. Parametron logic

The only successful alternative to the vacuum tube (before the transistor) was invented in Japan by Eiichi Goto in 1954. This ferrite unit was wound with varying numbers of coils (depending on the function required) which were driven by AC at about 2 MHz. Logic levels were defined by the output AC phase created by addition and subtraction of input phases.

Parametrons were more reliable than vacuum tubes but consumed more current and the generation of the 2 MHz driving signal remained a problem. Related devices were made in England and the USSR but they were not developed as far as in Japan.

3. Williams tube memory
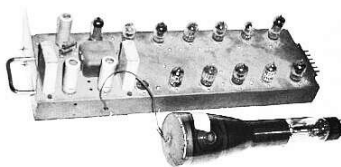
The invention of a practical electronic memory by Freddie Williams in 1948 at the University of Manchester made the modern computer possible. His device used a radar display tube and depended on the persistence of the phosphor *AND* that a wire mesh over the screen picked up a different signal depending on whether the electron beam struck a spot which was blank or which had recently been written. The main downside was that the whole store of about 1K bits had to be re-written 10 times each second. 40 tubes with support logic were used in most IAS machines ($^1/_{40}$ of SILLIAC's memory is illustrated).

4. Magnetic core memory

Tiny ferrite toroids (cores) were threaded with two insulated write wires and a sense wire. A pulse in each write wire generated *half* the magnetic field necessary to alter the magnetisation of cores. Where pulsed wires intersected in a core its magnetisation could be switched in either of two directions and a change would be detected by a pulse in the sense wire. No change could be 0 while a change indicated a 1, which would need to be immediately written back. This memory required considerable logic to select individual write wires.

5. Paper tape reader
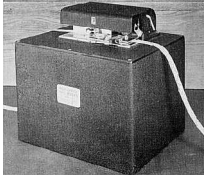
Most of the family loaded their programs and data from 5 channel paper tape. This 200 character per second optical reader from Ferranti UK was a frequent choice. Though the 5 channel (5 bit) Baudot coding was well known, the punch coding of its characters '0' to '9' were not binary numeric values 0 to 9. To simplify operations tape punches and printers were generally modified to an "IAS" code.

6. Paper tape punch
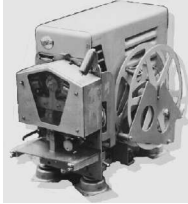
Not only was data output required for normal data processing but punches, such as this 100 character per second Teletype BRPE could punch more than twice as fast as printers could operate, so much of the printing was done "off line".

7 Printer
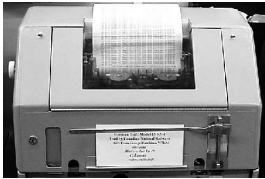
A considerable variety of printers were available from Teletype, Creed, STC (as shown) etc. They mostly printed at about 50 character per second and needed significant delays for carriage return and line feed! These were electro-mechanical devices - universally with awkward ribbons, mechanical character decoding that needed regular adjustment, and an aura of hot oil.

8. Magnetic tape
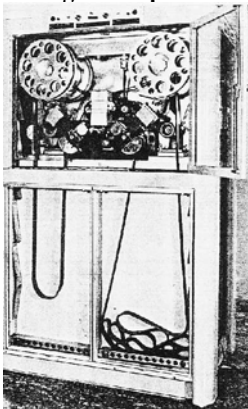
Some of the family added magtapes so as to support large data sets. There was no standard and systems varied from ¼ inch wide with 2 tracks to 2 inch 42 track units (with up to 2400 feet of tape), and to multi-spool carousels. This impressive drive was attached to ORACLE.   (ORNL photo)

9. Magnetic drum
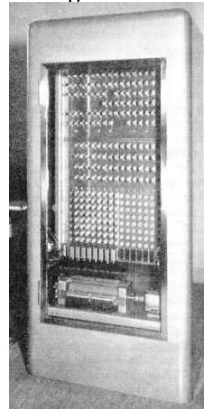
Some machines added fast drum memories - cylinders coated with iron oxide paint and accessed by fixed position heads. A few used a drum as the main memory. This drum comes from BESK, it has control logic in the top 80% of the window, a horizontal drum at the bottom left and a drive motor at the bottom right. A row of read/write heads sits at the top of the drum.   (Photo courtesy of Jan Karlqvist)

10. Simplified architecture of the IAS Computer
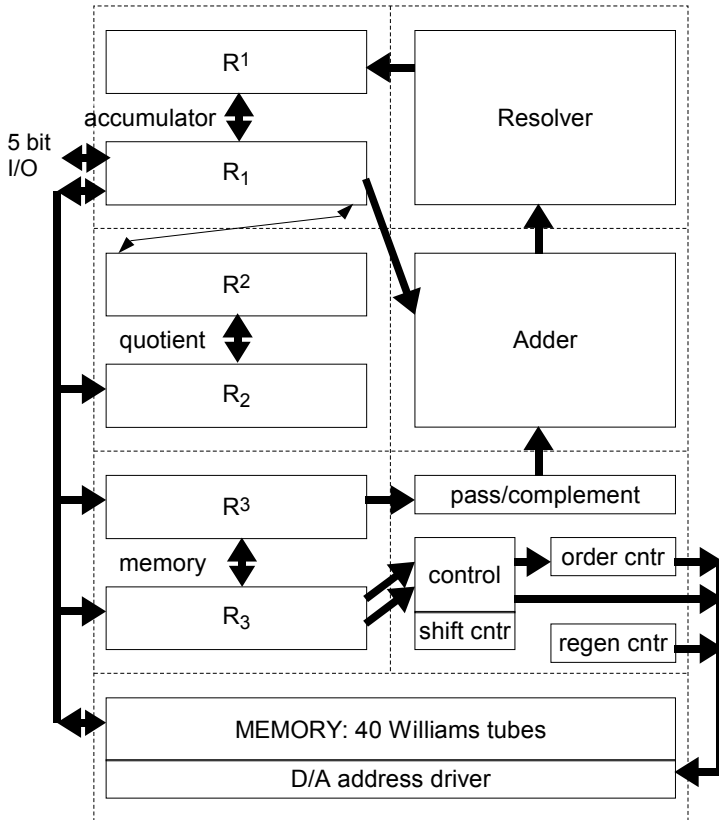
The dotted outline indicates the physical layout of the IAS Computer, end on.
- Broad arrows are parallel links, mostly 40 bits wide, and there is one single bit link.
- **R1, R2, R3** - the three logical 40 bit registers were each composed of "upper" and "lower" halves with a variety of interconnections for transfers or shifting.
- **Adder** - inputs were from the Accumulator and Memory via R_3. Subtraction was done via the **Complement** logic. The **Resolver** completed the Adder's carry process (many machines used an adder design without the Resolver).
- **Control** - used either the odd or even 20 bit instruction stored in R_3 to control operating signals and multi-stage instructions such as shift, multiply and divide.
- **Memory** - the 40 CRTs each provided one bit of a word. These had to be read and rewritten about 10 times a second under control of the **Regen** counter between instructions (some machines used different memory technology and many located the memory at the top). The **Control** logic provided memory addresses for instruction operands, and the **Order** counter provided the address of the next instruction pair. The 10 bit address was converted to voltages to position the tubes' reading electron beam.

Index

A teletype used with TRASK. It was known among Swedish programmers as *Dunderklumpen* (literally "thunder blob") - a children's book character who was very heavy and very noisy.
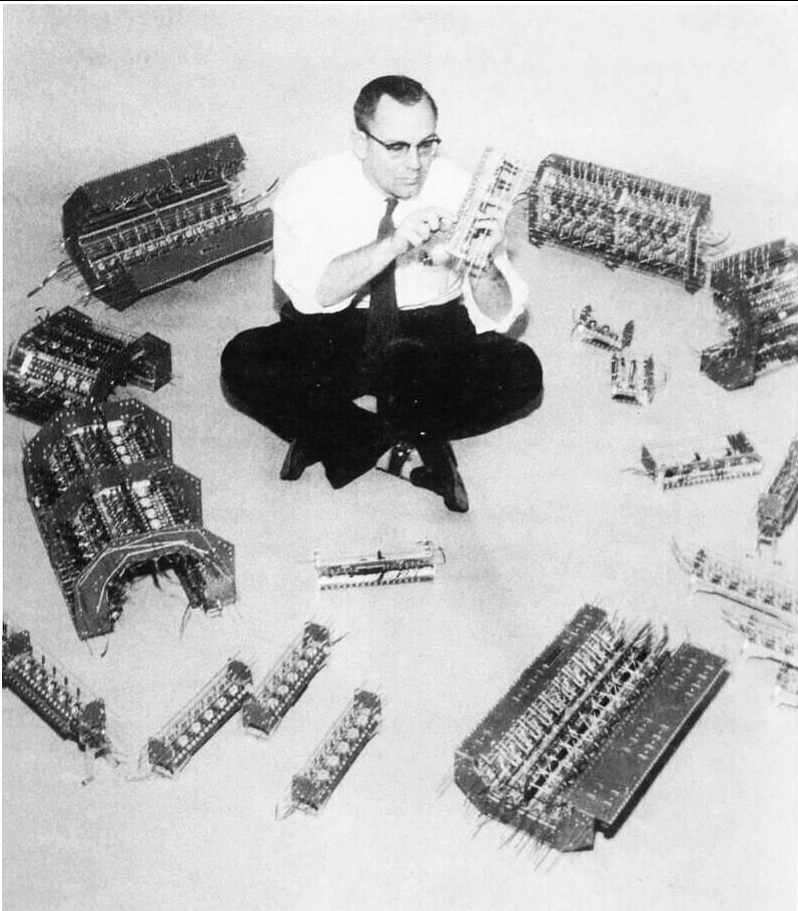
Typical IAS Computer family system components
Michigan State University's Dr Lawrence Von Tersch with bits of *MISTIC*

Between 1951 and 1965 John von Neumann's IAS design was copied by

Uni. Illinois	Los Alamos Nat.Lab	Argonne Nat.Lab	Rand Corp
Michigan State Uni	Iowa State Uni	Oak Ridge Nat.Lab	IBM Corp

Sweden's Royal Inst Tech	Lund Uni. Sweden	Denmark's Acad.Tech.Sci	Sydney Uni. Australia	Weizmann Institute Israel
Facit Sweden	SAAB Sweden	NTT Japan	Fujitsu Japan	*any more?*

These were the supercomputers of the first generation - an architecture based on 3,000 fragile glass radio tubes for the logic, and 40 WW2 radar display tubes to provide the first random access memory. They used every trick available in 1950 to get maximum performance.

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